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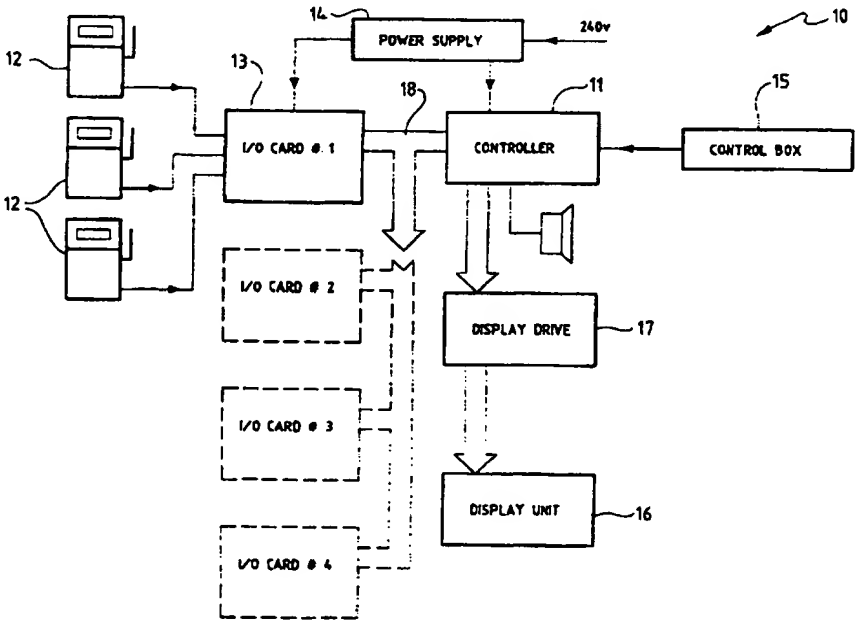
(57) Abstract

A jackpot controller (11) receives input signals from poker machines (12) via input/output (I/O) cards (13). Each I/O card (13) has 64 inputs, connected to respective poker machines (12). A counter (131) is provided for each input to count incoming pulses. The count is stored in a buffer (136) which is subsequently read by a microprocessor (110) within the controller (11). Unlike the polled port technique, the controller (11) is not required to spend the majority of time checking the inputs for signals from the poker machines. Every time a poker machine is played, the jackpot value is incremented and two random numbers are generated by the controller. The two numbers are compared and a jackpot win is triggered if the numbers match. The allowable range of the random numbers is progressively reduced so that a match is guaranteed by the time the jackpot reaches a predetermined maximum value.



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"GAMING APPARATUS"

THIS INVENTION relates to gaming apparatus. In particular, the invention is directed to an improved jackpot controller adapted to be linked to a plurality of gaming machines, such as those commonly known as poker machines or "fruit" machines.

This invention also relates to a random jackpot system, namely a method of determining which one of a plurality of gaming machines wins a progressive jackpot.

BACKGROUND ART

Typically, when playing a poker machine, the player receives a monetary reward (or credit) when one of a selected number of combinations appears on the machine's display. Many poker machines include a jackpot facility. That is, a certain percentage of the amount bet is allocated to a jackpot, which has a relatively high value and is payable when a particular combination is drawn or when a random event occurs. (There may be more than one jackpot).

Since the jackpot is derived from the money (or credit) input into that machine, the value and/or frequency of winning of a single machine jackpot is necessarily low.

To increase the value and/or frequency of jackpot winnings, and thereby make the poker machines more attractive to potential players, it is known to link several poker machines to a jackpot controller whereby all machines contribute to a jackpot which may be won by a player at any one of the contributing machines. In large gaming establishments having a large number of poker machines, a high value jackpot can be obtained, thereby providing increased enticement for players.

Known jackpot controllers are sold under the trade names MIKON SYSTEM and DAUMA SYSTEM. Other linked jackpot systems are described in Australian patents 268377 and 589158.

However, known jackpot controllers have some inherent disadvantages. For example, existing linked

controllers can only support a maximum of about 30 poker machines before further slave processors have to be used. That is, to connect say 40 machines, two complete controllers are required.

Existing controllers use a polled port approach, i.e. the input ports (connected to the individual poker machines) are read and any pulse at an input port is processed before the next pulse is received from the corresponding poker machine. If the controller cannot service an input port before the next pulse arrives, then the first (existing) pulse is overwritten and lost. This is one of the principal reasons why existing links are limited to a smaller number of machines per controller.

It is an object of the present invention to provide an improved jackpot control apparatus for gaming machines. In particular, it is an object of the invention to provide a controller which can support an increased number of poker machines.

There are various known methods of setting the jackpot value and determining which poker machine wins the jackpot. Some of these methods are based on the outcome of random events. Examples of such methods can be found in Australian patents nos. 268377, 524709 and 589158.

It is another object of the present invention to provide an alternative random jackpot system which is more attractive to the player and the gaming establishment operator, or which at least provides the operator with a useful choice.

SUMMARY OF THE INVENTION

In one broad form, the present invention provides a jackpot controller for gaming machines, comprising

a plurality of inputs each adapted to receive a signal from a respective gaming machine, and

a control circuit for processing the input signal information,

characterised in that the controller further comprising counting means associated with each input for counting the signals received from the respective gaming machines at that input.

Typically, the counting means is a four bit counter for each machine input. Each counter can store up to 16 pulses. The counters allow the pulse to be received and counted, even when the control circuit is not actually looking or waiting for them. The control circuit is therefore released of the time consuming task of continuously polling its inputs to see if pulses are present are not. This allows the control circuit to handle a higher number of inputs. In other words, a single jackpot controller can handle a higher number of gaming machines.

Typically, the gaming machines are poker machines. When each poker machine is played, it sends a signal to the jackpot controller.

Preferably, the inputs are grouped on cards. A card may typically contain 64 inputs. The jackpot controller comprises a plurality of input/output cards connectable to the control circuit.

In a preferred embodiment, up to four I/O cards, each containing 64 inputs, are connectable to a single control circuit, giving the control circuit a capacity of 256 machines. Thus, if the number of poker machines is increased from, say 50 to 100, it is not necessary to install a new jackpot controller. Rather, only an additional I/O card is required.

In another form, the present invention provides a method of random jackpot payment to one of a plurality of gaming machines, comprising the steps of

incrementing (or decrementing) a jackpot value from a first value towards a second value in predetermined steps in response to the playing of the gaming machines,

generating at least two random outputs in response to an incrementing (or decrementing) step,

comparing the two random outputs, and

triggering a jackpot win in the event that the random outputs are the same.

In yet another form, the present invention provides apparatus for random jackpot payment, comprising a control device connected to a plurality of gaming machines and having

means for incrementing (or decrementing) a jackpot value from a first value towards a second value at a predetermined rate in response to the playing of the gaming machines,

at least two random output generators, the random output generators being adapted to generate a respective random output in response to the incrementing (or decrementing) means,

comparator means for comparing the two random outputs, and

means for triggering a jackpot win if the random outputs are the same.

Typically, the gaming machines are poker machines.

Preferably, the current jackpot value is displayed to the players.

In a preferred embodiment of the invention, the jackpot value is incremented from the first value (which is the minimum jackpot value) towards the second value (which is the maximum jackpot value) every time one of the gaming machines is played, the increment typically being a proportion of the amount bet on that machine. At each increment, two random outputs are generated. The two random outputs are typically numbers generated by electronic random number generators. If the two random numbers are the same, the current jackpot value is allocated to the machine which caused the jackpot incrementing step that resulted in the generation of two matching random numbers. However, it will be apparent to those skilled in the art that the jackpot could be allocated to another machine bearing some relation to the

triggering event, e.g. the next machine played.

When the jackpot is won and paid, the jackpot value is reset to the first (minimum) value. An additional "residual" value may suitably be added to the minimum value, if desired. This residual value may be proportional to the amount bet on the gaming machines during the period between the triggering of the jackpot and the clearing or resetting of the jackpot.

Preferably, the range of the random outputs is limited, i.e. the random number generators are designed to randomly generate numbers within a specified range.

To ensure that a match occurs at some point before the current jackpot value reaches the maximum value, the range of numbers that the random number generators can produce is progressively reduced as the jackpot cycle continues. This ensures that a match will occur before the maximum value is reached.

In order that the invention may be more fully understood and put into practice, a preferred embodiment thereof will now be described with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram of a link progressive random jackpot system according to one embodiment,

Fig. 2 is a schematic block diagram of an input/output card of Fig. 1,

Fig. 3 is a circuit diagram for one input in the input/output card; and

Fig. 4 is a schematic block diagram of the controller card of Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in Fig. 1, the link progressive random jackpot system 10 (hereinafter referred to as "the link") comprises a controller 11 which is connected to several poker machines 12 (only 3 of which are shown) via an input/output (I/O) card 13. The link typically has four I/O cards, each connected to a number of poker machines

(not shown). A power supply 14 suitably provides regulated power for the circuitry of the controller 11, the input/output card 13 and the remaining components of the link 10.

All of the circuit cards or subsystems of the link 10 are typically housed in a single box, except for the poker machines 12, and an external control box 15 for the controller card 11.

The major operations of the link 10 are controlled by controller 11 which itself is software controlled. The controller 11 reads input pulses from the poker machines 12 (after processing through the input/output card 13), and responds to the input information by updating the jackpot display, triggering the jackpot and/or displaying audit information.

An I/O card 13 is shown in more detail in Fig. 2. The input stage of the I/O card includes a separate input for each poker machine. Typically, 64 inputs are provided on each I/O card. Pulses received from a meter on a poker machine 12 are fed to a respective input counter stage 131 via an input isolation stage 132 which typically contains an opto isolator circuit for each input. In the isolation stage, the incoming pulses are processed and converted to a level which the link can recognise and process.

The input counter stage 131 has counting circuits which count the pulses received from the respective poker machine 12, and store the count for use by the next stage. A counter is provided for each input.

The I/O card 13 is a slave circuit controlled by a master circuit in the controller 11. Commands are passed from the controller 11 to the I/O card 13 via a main data cable 18 which is the principal connection between the controller card and the I/O card. A bus buffering circuit 133 provides the interface between the data cable 18 and the I/O card. This bus buffering circuit is controlled by commands from the controller 11, and determines when data is to be transferred over the

main data cable 18.

An address decoding circuit 134 is connected to the bus buffering circuit 133 via the main bus 135 within the I/O card. The address decoding circuit 134 generates all the required control signals for the circuits on the I/O card, from the instructions received from the controller 11 via the data bus 18 and the I/O main bus 135.

An input buffer circuit 136 is used to read and clear the counters in the input counter stage 131, under instructions received from the controller 11 via the main control data bus 18 and the I/O main bus 135. Information read from the counters is fed back to the controller via the buses 135, 18.

Fig. 3 illustrates the input stage of the I/O card for a single gaming machine input (the other inputs being omitted for clarity). As mentioned above, the input isolation stage 132 includes an opto-isolator 132A at its input end, followed by a buffer 132B which provides an interface between the input isolation and the counter stage, and also provides pulse shaping. The count buffer 132B may be a suitable integrated circuit which can handle up to 8 separate inputs.

The outputs of the buffer are fed to respective 4 bit counters 131 in the counter stage. Thus each counter can count up to 15 input signals. If a counter is not read and reset by the controller before the count reaches 15, then a wrap around to zero will occur. However, this is unlikely to occur as the controller will service each counter typically before 2-3 counts. Each counter has two inputs, the first being the pulse received from the gaming machine via the isolation stage, and the second being used to reset the counter after the current count has been read by the controller.

The four output lines from the counter connected to a buffer circuit 136. The buffer circuit is typically an integrated circuit able to handle the four bit outputs of two counters. The buffer 136 provides a

buffer between the counter stage and the main controller data bus, and the content of the buffer circuit 136 can be read by the microprocessor 110.

In addition to receiving input signals from the machines 12 and the controller 11, the I/O card provides output display signals. Namely, in the event of a jackpot win, the I/O card sends signals to each participating machine, via an output latch stage 137 and output driver stage 138, to turn on lights on the machines indicating that a jackpot has been registered. The output latch stage receives the signal information from the main bus and, when required, will output signals to the output driver stage 138. The output driver 138 boosts the low level signal at its input to a suitable output level sufficient to drive the display lights.

The controller card 11 is used to control all the principal operations in the link 10 and is shown in more detail in Fig. 3. The core elements of the controller card 11 are a microprocessor 110, a memory 111 and an address decoding circuit 112 which are interconnected by a data/address bus 113.

The microprocessor 110 executes the control software which is contained in memory 111. The memory contains both RAM and ROM type memory. The ROM memory contains the program code, while the RAM stores working variables as well as other data that might need to be stored.

The RAM chips in the memory 111 are of two types, normal and battery-backed. The normal RAM chips are used for temporary storage of numbers and other data, as well as storage of the results of calculations and decisions made. The battery-packed RAM chips are used to store numbers and other data which are required to be retained in the event of a power failure. Such numbers/data include, for example, audit meter readings, current display values and the like.

The address decoding circuit 112 generates and controls data transfer between the various elements, and

provides synchronisation of the system components, e.g. by appropriate timing signals.

The controller 11 also includes a DUART circuit 114 which controls communications with devices external to the controller. Any information or data that is obtained by the link 10 from an external computer will pass through the DUART circuit. Additionally, any data that the link 10 transmits will also pass through the DUART circuit.

A communications isolation circuit 115 ensures that all incoming and outgoing data is suitably processed to make it compatible with the link or the outside device, as the case may be.

The display unit 16 (Fig. 1) of the link 10 also receives information via the DUART circuit 114. Typically, the type of information that is sent to the display unit 16 is updated jackpot display values and/or a control command to scroll or flash the display. The display unit 16 can also display audit information when required. This display can scroll through information from the meters on the respective poker machines 12, via suitable software control.

The DUART circuit 114 has an output connected to a jackpot level drive circuit 116. The jackpot level drive circuit, in turn, has one or more outputs each connected to a light, siren or other signalling device. When the DUART circuit 114 outputs a signal to the jackpot level drive circuit, it causes the lights, sirens or other signalling devices to function, thereby alerting supervisory persons that the jackpot has been triggered.

The controller 11 is controlled by an external control box 15 which typically comprises various manual or computer-controlled switches. The control box 15 is connected to a control box input circuit 117 inside the controller 11 which enables signals to pass to the main controller core, including the microprocessor 110. These signals may indicate to the link 10 that a service must be attended to. Such services typically include jackpot

clearing, audit meter reading, system checks, etc.

As mentioned above, the I/O card 13 is controlled by the controller 11. All communications between the controller 11 and I/O card 13 pass through an address & data bus interface 118, which is controlled by the microprocessor 110 to enable the appropriate information and commands to be sent/received to/from the I/O card 13.

Typically, an 8 bit microprocessor, such as a 68HC11A1 microprocessor is used. With 8 bit communications, a total of 256 poker machines can be connected to the link. Each I/O card 13 provides the direct interface between the controller card 11 and up to 64 poker machines. The link 10 may contain four I/O cards, giving a total capacity of 256 machines connected at one time.

The input counter stage 131 contains a four bit counter for each poker machine input. The respective counter is incremented on receipt of the appropriate signal from the poker machine. Each counter can store up to 16 pulses before overflowing, thereby allowing the microprocessor ample time to read the counter values from the input buffer stage 136. In other words, the controller 11 can perform all the other required tasks without having to spend the majority of its time checking the inputs (as required in the polled approach). The input counters will be read when the processor is free of other tasks. In practice, the controller will normally be able to access each counter within 1-3 pulses. The ability to store 16 pulses therefore provides a comfortable safety margin, ensuring that machine pulses will never be missed or lost and maintaining correct reconciliation of customer cashflow.

The counters allow the pulses to be received and counted, even when the controller is not actually looking or waiting for them. The controller is therefore released of the time consuming task of continuously scanning its inputs to see if pulses are present or not.

Instead, a loop is sequentially performed by which the controller does block transfers of a group of counters. The count values are then processed in a quick and efficient manner in an inner loop within the microprocessor. The counters can be enabled or disabled by the microprocessor at any time, as required. They can also be reset in banks of eight for a clear start of the process.

In use, whenever a machine is played, its meter will transmit a signal to the I/O card to which it is connected. This signal is fed to the controller where it is processed. Typically, the jackpot will be incremented with each signal from a poker machine.

After some internal processing which may or may not depend on random events, the controller will decide if the signal from the poker machine triggers a jackpot event. If it does, the relevant alarm will be sounded, and the display unit 16 will flash or otherwise indicate that the jackpot has been won. For example, when the jackpot is triggered, large display signs will show the jackpot level and value alternatively. The controller will also cause the light and/or alarm on the poker machine which triggered the jackpot to be activated, thereby notifying the player of the jackpot event.

To resume normal operation, the jackpot is cleared, and reset at the desired level.

The abovedescribed apparatus can be used to implement the random jackpot method of this invention. However, any other suitable jackpot apparatus can be used for the method.

In such random jackpot apparatus, a jackpot controller is connected (either hardwired or by radio signal) to a number of poker machines. The jackpot controller is also connected to a display which displays the current jackpot value. When a poker machine is played, a signal is sent to the jackpot controller. This signal normally contains information relating to the amount bet.

At the start of each jackpot cycle, the jackpot value is set at a predetermined minimum value, known as the startup value. Hence, on initial startup the display will show the startup value. Similarly, the display will return to this startup value when the jackpot is reset after a win.

Whenever a poker machine is played, the displayed jackpot value will be incremented at a predetermined rate. This rate is usually set as a percentage of machine turnover, and is derived from the signal pulses sent from the participating machines to the jackpot controller. For example, if the increment rate is set at 10%, the display will increase by 10 cents for every dollar played on each machine.

Each time the jackpot value is incremented, two independent random number generators each produce an output number, and the two output numbers are compared. If a match occurs, i.e. the two output numbers are the same, the jackpot is triggered at this point (known as the trigger point). The jackpot is typically allocated to the poker machine which caused the increment which resulted in the generation of two matching random numbers. (However, the jackpot might be allocated to some other machine bearing some relation to the trigger point, e.g. the next machine which causes an increment in the jackpot value). The value of the jackpot allocated to the winning machine is the value displayed at the trigger point.

If the two randomly generated numbers do not match, the jackpot cycle is repeated the next time a machine is played, with the jackpot value again being incremented towards the predetermined maximum value. The maximum value is the maximum amount that the jackpot can reach, and the jackpot must trigger before this value is reached.

To ensure that a match occurs between the randomly generated numbers at same point before the displayed jackpot value reaches the predetermined maximum

value, the allowable range of numbers that the random number generators can produce is progressively reduced as the jackpot cycle continues. Initially, each random number generator will generate an output number between, say, 1 and a maximum range number that may be either set manually or controlled by software. This maximum range number sets the output range of the random number generator, and hence the likelihood that the two random output numbers will be the same. For example, if the maximum range number is set at 20, then the random number generator can only output a (integer) number from 1 to 20, inclusive.

The initial output range of the random number generators is determined by the minimum (startup) value and the maximum value, both of which are predetermined. Typically, if the display increments in cent steps, the initial output range of the random number generators will be the number of cents between the startup value and the predetermined maximum value. For example, a jackpot controller having a startup value of $100 and a predetermined maximum value of $200, will have an initial output range of 10,000. In the first cycle, each random number generator may produce a number within the range of 1 to 10,000.

Thereafter, the allowable output range will be reduced on each jackpot cycle. Typically, the allowable output range will be reduced by 1 for each cent by which the displayed jackpot value is incremented. In a worst case situation, if no match has occurred before the jackpot value reaches the predetermined maximum value, the allowable output range of each random number generator will be 1, and a match is therefore guaranteed from the resultant 1:1 comparison.

The likelihood that the jackpot will be won increases during the jackpot cycle. That is, it is less likely that the jackpot will be won early. This means that the jackpot is likely to increase, and thereby add to the suspense or anticipation of a jackpot payout.

After a jackpot has been triggered and paid, the jackpot is reset, normally to the startup value. However, a "residual" value may be added to the reset jackpot value. This residual value is a proportion, based on the increment rate, of the money bet in the poker machines between the trigger point and the resetting of the jackpot. This value is determined from the pulses that were received by the jackpot controller while the jackpot was waiting to be cleared. That is, once a jackpot has been triggered, the displayed value will remain static until cleared by an attendant. Any pulses received from the individual machine during this period will be stored and added to the startup value at the beginning of the next jackpot cycle.

The method is suitably implemented in computer software, using either hardware or software random number generators and comparator.

The foregoing describes only one embodiment of the invention, and modifications which are obvious to those skilled in the art may be made thereto without departing from the scope of the invention.

For example, the gaming machines need not be poker machines; they may be other gaming or amusement machines.

Further, the jackpot win may be made dependent on the outcomes of more than two random event generators.

CLAIMS

1. A jackpot controller for gaming machines, comprising

a plurality of inputs each adapted to receive a signal from a respective gaming machine, and

a control circuit for processing the input signal information,

characterised in that the controller further comprises counting means associated with each input for counting the signals received at that input.

2. A controller as claimed in claim 1, wherein the counting means comprises an electronic counter circuit.

3. A controller as claimed in claim 2, wherein the counter is a four bit binary counter.

4. A controller as claimed in claim 1, further comprising an isolation circuit between each input and its associated counting means.

5. A controller as claimed in claim 1, further comprising a buffer circuit connected to each counting means and adapted to read the signal count, and means for resetting the signal count.

6. A controller as claimed in claim 1, wherein the inputs are grouped on input/output cards, each card being connected to the control circuit.

7. A controller as claimed in claim 6, comprising four input/output cards, each having 64 inputs thereon.

8. A controller as claimed in claim 1, wherein the control circuit comprises a microprocessor.

9. A controller as claimed in claim 1, wherein the gaming machines are poker machines.

10. A controller as claimed in claim 1, further comprising signalling means, responsive to a jackpot win by one gaming machine, for transmitting signals to all other gaming machines connected to the controller.

11. A controller as claimed in claim 10, further comprising means for actuating one or more audio and/or visual alarm(s) in the event of a jackpot win.

12. A control circuit for gaming machines,

comprising

a plurality of inputs each adapted to receive a signal from a respective gaming machine,

characterised in that the control circuit further comprises a counter at each input for counting the signals received at that input, and means for reading and resetting the count of each counter.

13. A method of random jackpot payment to one of a plurality of gaming machines, comprising the steps of

incrementing (or decrementing) a jackpot value from a first value towards a second value in predetermined steps in response to the playing of the gaming machines,

generating at least two random outputs in response to an incrementing (or decrementing) step,

comparing the two random outputs, and

triggering a jackpot win in the event that the random outputs are the same.

14. A method as claimed in claim 13, wherein the jackpot value is incremented from the first value towards the second value each time a gaming machine is played, the incremental step being a proportion of the amount played.

15. A method as claimed in claim 13, wherein the two random outputs are numbers within a predetermined range.

16. A method as claimed in claim 15, wherein the range of the random numbers is progressively reduced with each step, until a match occurs between the two generated random numbers.

17. A method as claimed in claim 13, further comprising the step of resetting the jackpot value to a predetermined value after a jackpot win.

18. A method as claimed in claim 13, further comprising the step of allocating the jackpot win to a gaming machine bearing a relationship to the triggering event.

19. Apparatus for random jackpot payment,

comprising a control device connected to a plurality of gaming machines and having

means for incrementing (or decrementing) a jackpot value from a first value towards a second value at a predetermined rate in response to the playing of the gaming machines,

at least two random output generators, the random output generators being adapted to generate a respective random output in response to the incrementing (or decrementing) means,

comparator means for comparing the two random outputs, and

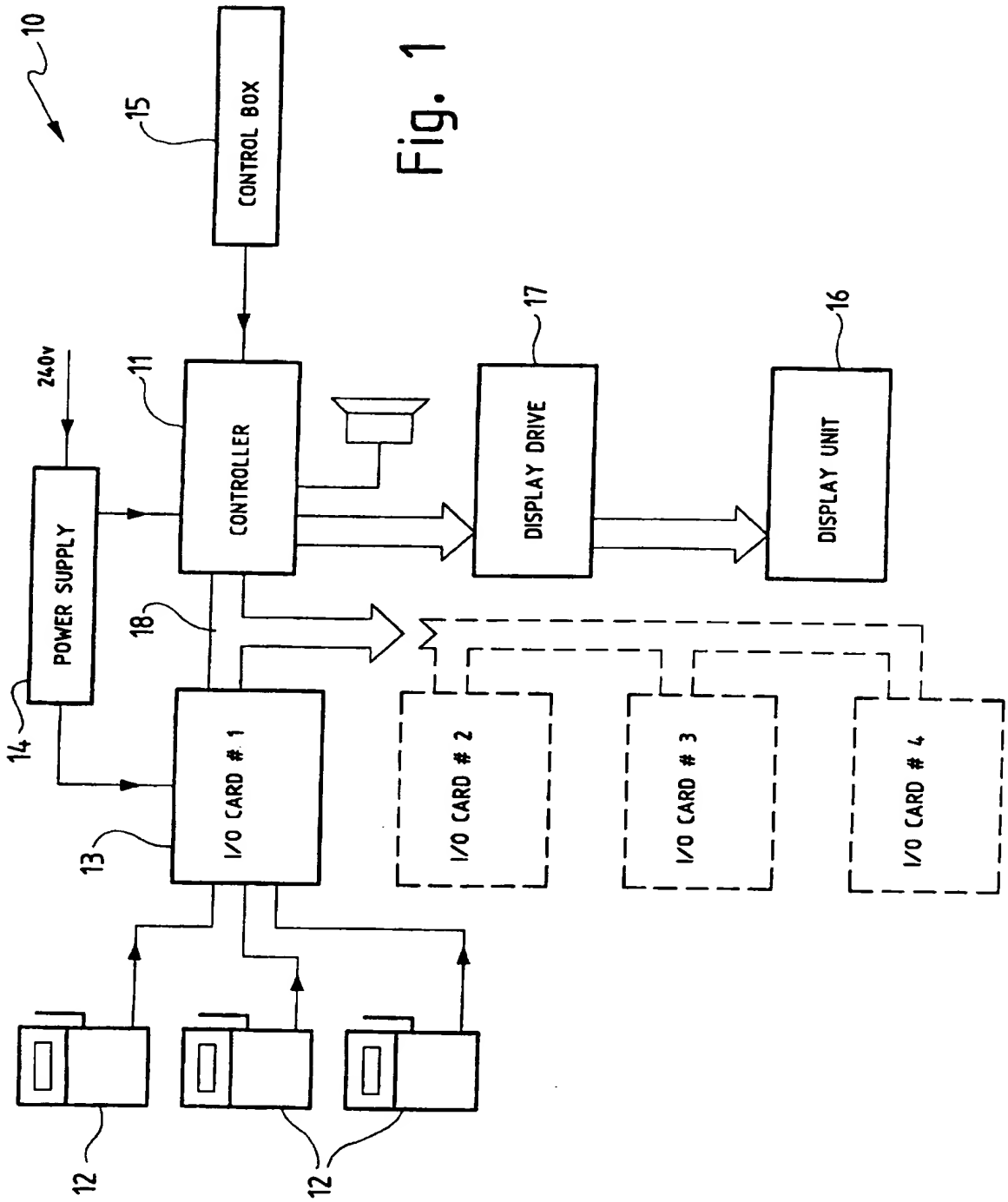
means for triggering a jackpot win if the random outputs are the same.

20. Apparatus as claimed in claim 19, wherein each random output generator is an electronic random number generator.

21. Apparatus as claimed in claim 20, further comprising means for progressively limiting the range of random numbers able to be generated by each random number generator.

22. Apparatus as claimed in claim 19, further comprising display means for displaying the current jackpot value.

23. Apparatus as claimed in claim 19, wherein the gaming machines are poker machines.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DISPLAY UNIT
POWER SUPPLY
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I/O CARD # 4
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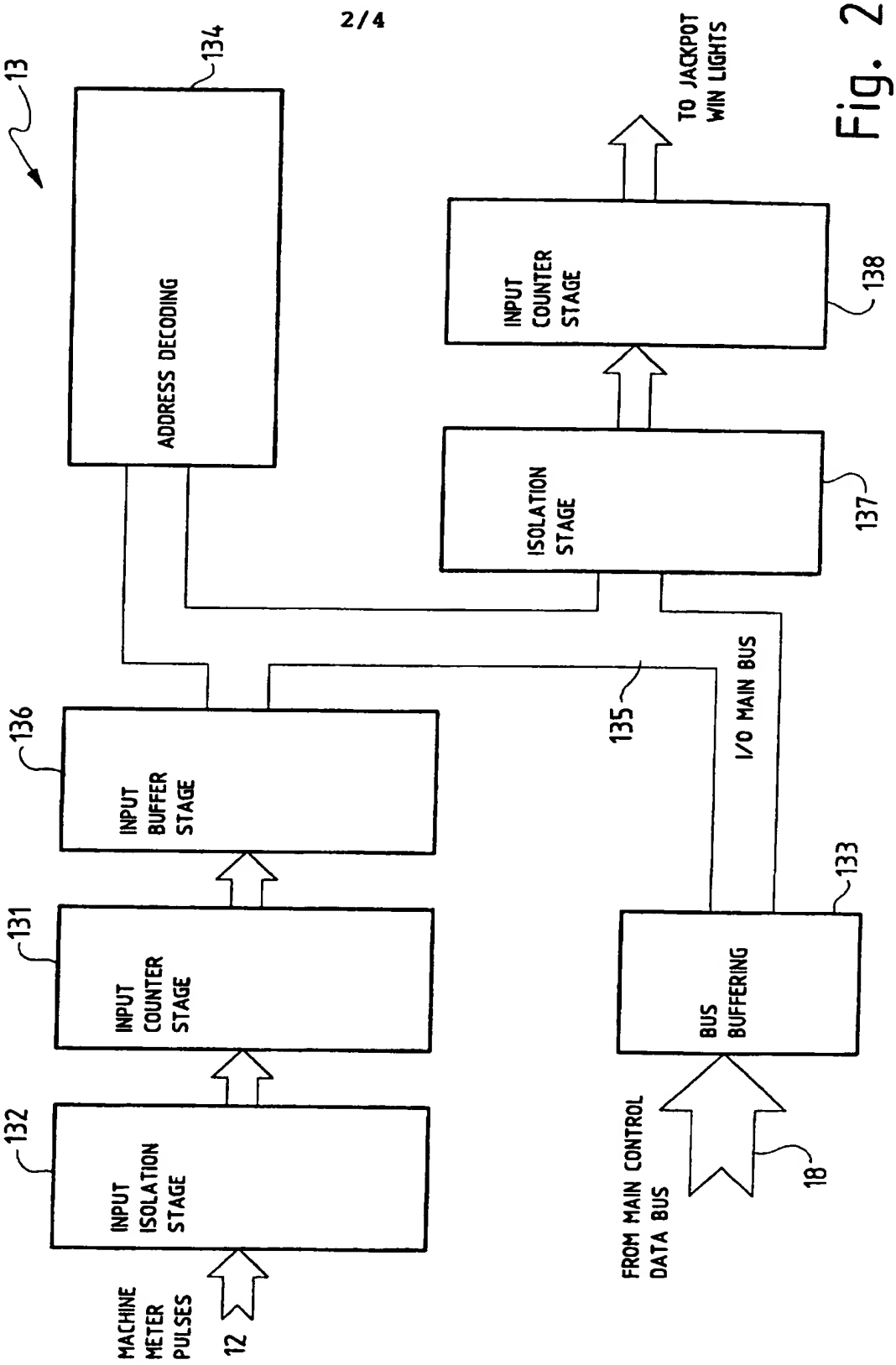
12
12

Fig. 1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INPUT BUFFER STAGE
131
INPUT COUNTER STAGE
133
BUS BUFFERING
132
INPUT ISOLATION STAGE
MACHINE METER PULSES
12
FROM MAIN CONTROL DATA BUS
18

Fig. 2

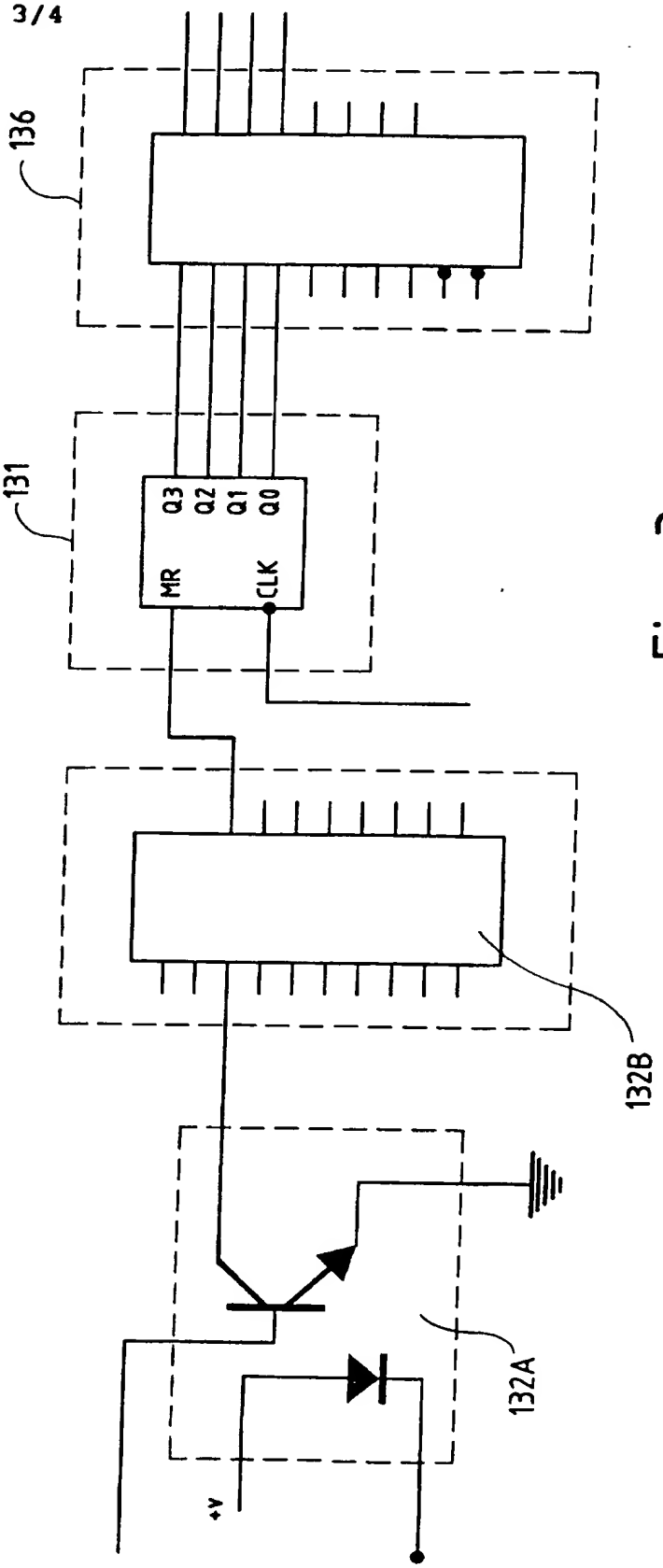

Fig. 3

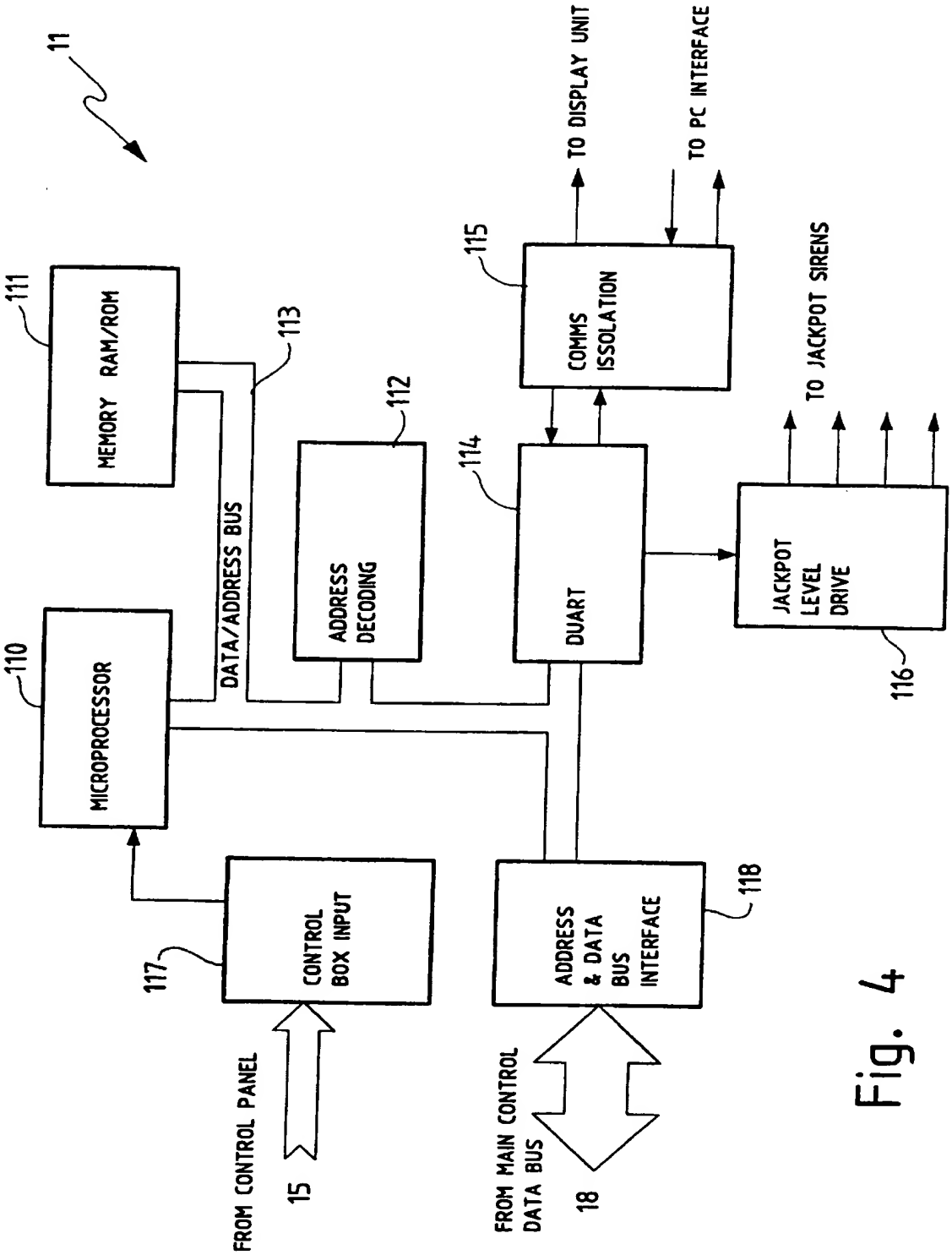
11
MEMORY RAM/ROM
111
113
DATA/ADDRESS BUS
112
ADDRESS DECODING
110
MICROPROCESSOR
115
COMMS ISSOLATION
TO DISPLAY UNIT
TO PC INTERFACE
114
DUART
TO JACKPOT SIRENS
JACKPOT LEVEL DRIVE
116
117
CONTROL BOX INPUT
FROM CONTROL PANEL
15
118
ADDRESS & DATA BUS INTERFACE
FROM MAIN CONTROL DATA BUS
18

Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 97/00031

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: G07F 17/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: G07F 17/34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DERWENT: 1. Control, controller, regulat:, governer, and 2. Count
JAPIO: as above

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	AU 53370/86 (589158) B (FRANKOVIC and FAZZOLARE) 14 August 1986 page 4, lines 9-27, Fig 1	1-3, 6-9
X	AU 39363/78 A (LAURIE) 6 March 1980 page 2, line 11 - page 3, line 27 page 4, line 17 - page 5, line 22 page 6, line 26 - page 9, line 5, Figs 1, 3	1-3, 6-9
A	AU 39181/63 (268377) B (FOSTER) 23 June 1966	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 1997	03.04.97
Name and mailing address of the ISA/AU AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA Facsimile No.: (06) 285 3929	Authorized officer M.E. DIXON Telephone No.: (06) 283 2194

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 97/00031

C (Continuation) **DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2165386 A (BARCREST LIMITED) 9 April 1986 abstract	
A	GB 2139390 A (AINSWORTH NOMINEE PTY LTD) 7 November 1984 page 1, lines 27-36, 54-58, Fig 1	
A	EP 0342797 A (KABUSHIKI KAISHA UNIVERSAL) 23 November 1989 Col 3, line 32 - col 5, line 5, Figs 1, 2	

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 97/00031

Box I **Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box II **Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1. Claims 1-12 are directed to a jackpot controller for gaming machines. The controller has a control circuit for processing input information from each gaming machine and counting means associated with each input for counting signals received at that input. It is considered that counting means associated with each input for counting the signals comprises a first "special technical feature".

2. Claims 13-23 are directed to a method or apparatus of random jackpot payment comprising incrementing (or decrementing) a jackpot value in response to playing of gaming machines. Generating at least two random outputs in response to an incrementing (or decrementing) step, comparing and then triggering a jackpot win in the event they are the same is considered to comprise a second "special technical feature".

Since the above-mentioned groups of claims do not share the technical features identified, a "technical relationship" between the inventions as defined in PCT Rule 13.2 does not exist. Accordingly the international application does not relate to one invention or to a single inventive concept

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-12

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

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This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
GB	2139390	AT	1451/84	AU	27572/84	DE	3416229
		ES	531967	JP	59-209374	NL	8401380
		US	4636951	ZA	8403276		
EP	342797	AT	112082	AU	33868/89	JP	1288289
		US	4964638				

END OF ANNEX